

Name.....Pnr.....

Exam, Computer Architecture 1DT157
Thursday 03/06/2004 at 8:30 am - 10:30 am

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Important information about this exam:

Answer every question with at most two sentences of normal length. Most questions can have even shorter answers, and some can be answered in a single word. Too long answers will mean a reduced score since what is being tested here is also the ability to discern relevant information.

Write your answer in the space immediately below each question. Do **not** use a separate sheet for answers.

Answers to open questions (of type "what is..." or "explain how...") must demonstrate an understanding beyond spelling out acronyms. For example, if the question is "What is DMA" the answer "Direct Memory Access" gets 0 points.

You may answer in English or in Swedish.

Note that there are questions on both sides of the sheets and that the exam begins on the other side of this sheet.

Each question can give at most 1 point. There are 30 questions in all. A pass requires 20 points, and an extra credit towards a higher grade requires 25 points.

Good luck!

1. What is the difference between **bit rate** and **baud rate**?

2. The **DMA** unit may steal cycles on the bus. Why?

3. Which of the following can be connected directly to the **PCI bus**? (Circle those you think are correct).

ALU ISA bridge control store mouse CRT display

4. Name three differences between **RISC** and **CISC** architectures.

5. What is the function of a **bus transceiver**?

6. In four bit **two's complement**, what is 0xa?

7. What in a floating point number is a **mantissa**?

8. What is meant by **temporal locality** in connection with cache memories?

9. For what purpose does the DMA unit use **interrupts**?

10. What is the difference between **write back** and **write through**?

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11. What does a **demultiplexer** do?

12. The laser in a **CD-RW** can operate at three different power levels, the lowest of which is used for reading. For what are the other two levels used?

13. How many bits are transferred in parallel on the **USB** bus?

14. What is the **fetch-execute cycle**?

15. Explain how **memory mapped I/O** works.

16. What is the difference between an **opcode** and an assembly instruction?

17. A machine like **IJVM** has the instruction “add” for adding two numbers. Which two numbers will be added by this instruction?

18. Which is the least number you can represent with **excess 128**? (answer in decimal)

19. Which of the following operations are normally performed by the ALU? (Circle those you think are correct).

Memory read Branch prediction Integer comparison Instruction decoding

20. How does one program a **PLA**?

21. Explain how **frequency modulation** works.

22. Suppose a hard disk stopped rotating. Would the **disk head** then be able to read the bit located immediately under it? Motivate your answer briefly.

23. What can cause a **RAW** dependence?

24. What is **EPIC**?

25. What does “unified” mean when we talk about a **unified cache**?

26. A hard disk has just accessed a set of data and is now requested to access another set located at the same **cylinder**. What is the seek time and why?

27. Why is the **LRU** replacement policy not necessary in a direct-mapped cache?.

28. If you increase the number of stages in a **pipeline** the performance of the CPU may go up. Why?

29. The major advantage of a **von Neumann machine** over its predecessors concerns the representation of the program. What was von Neumann’s key insight in this respect?

30. Explain a simple and useful strategy for **branch prediction**.

31. In the game of **Control**, which piece is fastest?